What is claimed is:

1. A data processing apparatus capable of implementing an execution of a virtual machine instruction based on an execution routine specified by a native instruction of a CPU, comprising:

an address converting unit capable of sequentially converting an address output from the CPU into an address of the native instruction by utilizing an address of a prepared execution routine in response to an application of a prescribed condition,

the address converting unit reading a virtual machine instruction to be executed next and preparing an address of an execution routine corresponding thereto in parallel with an execution of the execution routine by the CPU based on the address of the native instruction which is sequentially converted.

2. The data processing apparatus according to claim 1, wherein the address converting unit exactly outputs an address input from the CPU in response to a non-application of the prescribed condition.

3. The data processing apparatus according to claim 1, wherein the prescribed condition is an output of a predetermined address by the CPU.

4. The data processing apparatus according to claim 3, wherein the predetermined address is a starting address of a predetermined address space assigned to the execution of the

virtual machine instruction.

5. The data processing apparatus according to claim 4, wherein the execution routine includes a native instruction of a return processing of returning a program counter of the CPU to a head of the predetermined address space assigned to the execution of the virtual machine instruction at an end thereof.

6. The data processing apparatus according to claim 1, further comprising a conversion table for defining a correspondence of an instruction length to an address of an execution routine for each virtual machine instruction.

7. The data processing apparatus according to claim 6, further comprising a first register for holding an instruction length acquired from the conversion table corresponding to a virtual machine instruction and a second register for holding an address of an execution routine which is acquired.

8. The data processing apparatus according to claim 7, wherein the address converting unit has a virtual machine program counter for outputting an address to read a virtual machine instruction from a memory and an amount of an increment of the virtual machine program counter can be controlled based on a value of the first register.

9. The data processing apparatus according to claim 8, wherein the increment of the virtual machine program counter is carried out synchronously with an execution end timing of

an execution routine.

10. The data processing apparatus according to claim 7, wherein the address converting unit has an execution routine address generating circuit for reading a native instruction of an execution routine from a memory, and

the execution routine address generating circuit has a third register for inputting an address of an execution routine held by the second register and an adder for adding a value of the third register to a plurality of bits on a low order side of an address output from the CPU, and an output of the adder is set to be an address of a native instruction of an execution routine.

11. The data processing apparatus according to claim 1, wherein when a virtual machine instruction which is read is a branch instruction, the address converting unit can read a virtual machine instruction of a branch destination and can prepare an address of an execution routine corresponding thereto.

12. The data processing apparatus according to claim 1, wherein when a virtual machine instruction which is read is a conditional branch instruction, the address converting unit further reads a virtual machine instruction of a branch destination and separately prepares an address of an execution routine corresponding thereto, and selects an address of an execution routine to be utilized for an address conversion

depending on a presence of a branch.

13. The data processing apparatus according to claim 1, further comprising a first memory for storing a virtual machine program constituted by a virtual machine instruction and a second memory for storing an execution routine thereof for each virtual machine instruction, the data processing apparatus being formed on a semiconductor chip.

14. The data processing apparatus according to claim 13, wherein the second memory further has an instruction length of a virtual machine instruction.

15. The data processing apparatus according to claim 13, wherein the first memory is a rewritable non-volatile memory.

16. An IC card having an input/output circuit and a data processing apparatus connected to the input/output circuit on a card board,

wherein the data processing apparatus can implement an execution of a virtual machine instruction by an execution routine specified by a native instruction of a CPU and has an address converting unit for sequentially converting a predetermined address output from the CPU into an address of the native instruction by utilizing an address of an execution routine which is prepared,

the address converting unit reading a virtual machine instruction to be executed next and preparing an address of an execution routine corresponding thereto in parallel with

an execution of an execution routine by the CPU based on the address of the native instruction which is sequentially converted.